

NEZHA3 DKB V2R0_A (WITH LCD VERSION)

FUNCTION DIAGRAM

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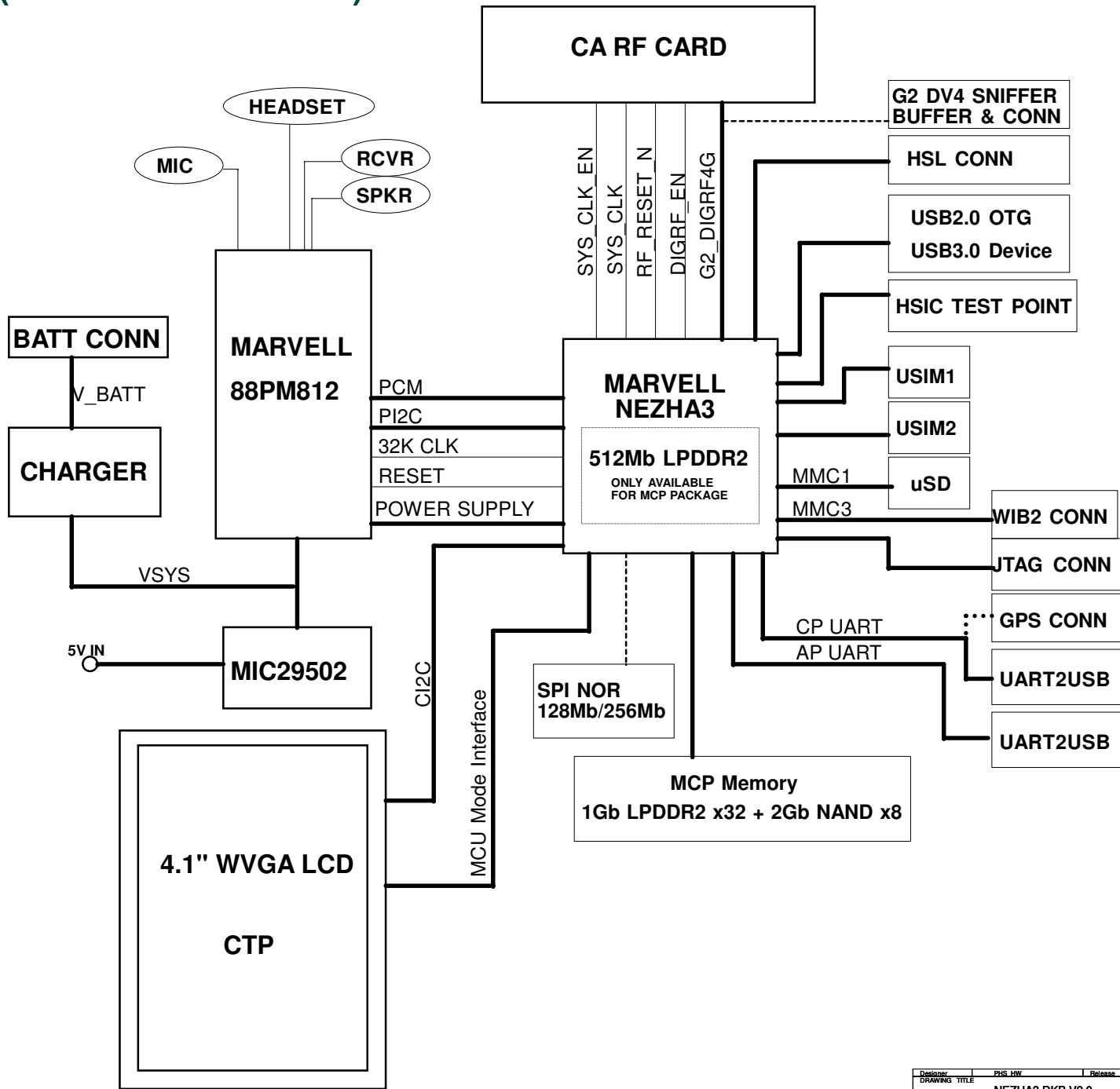
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VERSION HISTORY

VERSION	DATE	DESCRIPTION
1.0	2014.05.23	
2.0	2015.1.15	Design for Z3 stepping

RELEASE



DESIGNER	PHS_HW	Release	2015.01.15
DRAWING TITLE	NEZHA3 DKB V2.0		
SIZE	DOC NO.	RD-PHS-HW-SCH000000	Rev 1.0
A2	PCB NO.	PCB000000	LAST UPDATE Thursday, January 15, 2015
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GPIO/POWER/CLOCK TABLE

GPIO

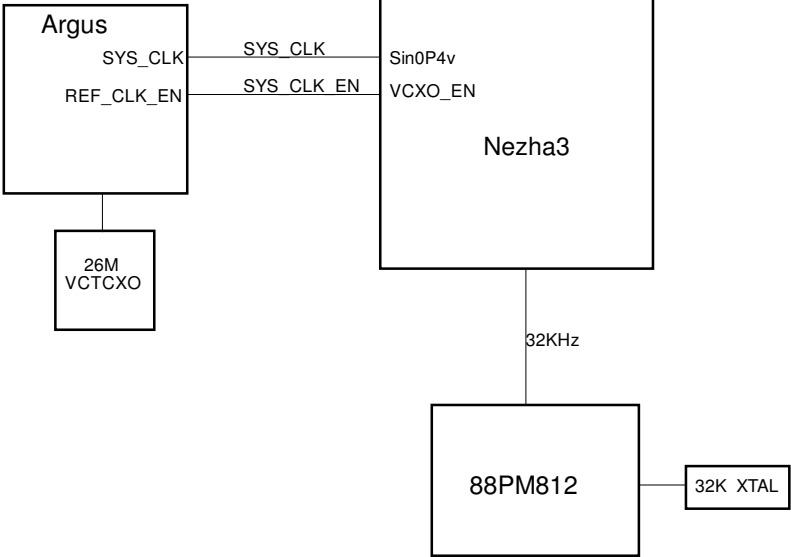
Diferent with NEZHA3 DKB 1.0				
Board		Nezha3 DKB V2.0		
Pad Name	Reset State	Usage	Function	FUNC 0-7
TDS_CLK	Low	MMC3_CMD	MMC3_CMD	4
TDS_DIO0	Low	WLAN_RSTn	GPIO[67]	1
TDS_DIO1	Low	WLAN_PdN	GPIO[68]	1
TDS_DIO2	Low	LTEWLAN_COEX_UART_IN	Ism_uart_in	5
TDS_DIO3	Low	LTEWLAN_COEX_UART_OUT	Ism_uart_out	5
TDS_DIO4	Low	MMC3_DAT[3]	MMC3_DAT[3]	4
TDS_DIO5	Low	MMC3_DAT[2]	MMC3_DAT[2]	4
TDS_DIO6	Low	MMC3_DAT[1]	MMC3_DAT[1]	4
TDS_DIO7	Low	MMC3_DAT[0]	MMC3_DAT[0]	4
TDS_DIO8	Low	MMC3_CLK	MMC3_CLK	1
TDS_DIO9	Low	TP_RESET	GPIO[77]	1
TDS_LNACTRL	Low	LCD_TE	GPIO[55]	1
TDS_MIXCTRL	Low	LCD_PWM	GPIO[56]	1
TDS_PACTRL	Low	DVC0	DVL0	2
TDS_PAON	PULL_DOWN	DVC1	DVL1	2
TDS_RXON	PULL_DOWN	GPS_RESET_N	GPIO[80]	1
TDS_RXREV	Low	UART2_TXD	UART2_TXD	6
TDS_TRXSW	Low	UART2_RXD	UART2_RXD	6
TDS_TXON	PULL_DOWN	AUX_CLK2_EN	GPIO[81]	1
TDS_TXREV	Low	GPS_ON_OFF	GPIO[59]	1
GPIO[60]	PULL_UP	DIGRF_EN	GPIO[60]	0
GPIO[61]	PULL_UP	HSL	HSL	5
GPIO[62]	PULL_UP	HSL	HSL	5
GPIO[63]	PULL_UP	HSL	HSL	5
GPIO[64]	PULL_DOWN	HSL	HSL	5
GPIO[65]	PULL_DOWN	HSL	HSL	5
GPIO[66]	PULL_UP	HSL	HSL	5
RF_CONT_4	Low	NC	GPIO[13]	6
PA_MODE	Low	GPS_PPS	GPIO[12]	6
ANT_SW4	Low	GPS_TIMER_SYNC	GPIO[11]	6
VCKO_REQ	PULL_DOWN	BT_WAKE_HOST	GPIO[125]	1
CLK_REQ	PULL_DOWN	TP_INT	GPIO[123]	1
MMC1_CLK	PULL_DOWN	MMC1(SD)	MMC1	0
MMC1_CMD	High	MMC1(SD)	MMC1	0
MMC1_DAT[0]	High	MMC1(SD)	MMC1	0
MMC1_DAT[1]	High	MMC1(SD)	MMC1	0
MMC1_DAT[2]	High	MMC1(SD)	MMC1	0
MMC1_DAT[3]	High	MMC1(SD)	MMC1	0
MMC1_DAT[4]	High	NC	GPIO[22]	1
MMC1_DAT[5]	High	NC	GPIO[21]	1
MMC1_DAT[6]	High	NC	GPIO[20]	1
MMC1_DAT[7]	High	NC	GPIO[24]	1
MMC1_CD	PULL_UP	MMC1_CD	GPIO[23]	1
GPIO[25]	PULL_UP	PCM_CLK	GPIO[25]	0
GPIO[26]	PULL_UP	PCM_SYNC	GPIO[26]	0
GPIO[27]	PULL_UP	PCM_TXD	GPIO[27]	0
GPIO[28]	PULL_UP	PCM_RXD	GPIO[28]	0
GPIO[33]	PULL_UP	CHG_PSEL/CP_WAKE_AP	GPIO[33]	0
GPIO[34]	PULL_UP	WLAN_WAKE_HOST/AP_WAKE_CP	GPIO[34]	0
GPIO[35]	PULL_UP	LCD_RST/CP_WDT	GPIO[35]	0
GPIO[36]	PULL_UP	USB_SEL/CP_ASSERT	GPIO[36]	0
GPIO[49]	PULL_UP	CHG_INT/AP_HSIC_RDY	GPIO[49]	0
GPIO[50]	PULL_UP	CHG_STAT/CP_BOOT_ACK	GPIO[50]	0
GPIO[51]	PULL_UP	UART1_RXD	UART1_RXD	1
GPIO[52]	PULL_UP	UART1_TXD	UART1_TXD	1
GPIO[53]	PULL_UP	CI2C_SCL	CI2C_SCL	2
GPIO[54]	PULL_UP	CI2C_SDA	CI2C_SDA	2
GPIO[124]	PULL_DOWN	CODEC_INT	GPIO[124]	0

Diferent with NEZHA3 DKB 1.0				
Board		Nezha3 DKB V2.0		
Pad Name	Reset State	Usage	Function	FUNC 0-7
ND_CS1n/SM_CS3n	HIGH	LCD_RESETn	GPIO[86]	1
ND_RDY1	PULL_UP	LCD_D13	LCD_D13	4
SM_SCLK	Low	LCD_WRn	LCD_WR	7
SM_RDY	PULL_UP	LCD_D11	LCD_D11	4
SM_CS0n	HIGH	LCD_RDn	LCD_RD	7
SM_CS1n	HIGH	LCD_CSn	LCD_CS0	2
SM_BE0n	PULL_UP	LCD_DATA/CMD	LCD_A0	5
SM_BE1n	PULL_UP	LCD_D15	LCD_D15	5
SM_ADV	PULL_UP	LCD_D14	LCD_D14	5
SM_ADV_MUX	PULL_UP	LCD_D12	LCD_D12	4
EM_DAT0 / GPIO[37]	PULL_UP	LCD_D0	LCD_D0	1
EM_DAT1 / GPIO[38]	PULL_UP	LCD_D1	LCD_D1	1
EM_DAT2 / GPIO[39]	PULL_UP	LCD_D2	LCD_D2	1
EM_DAT3 / GPIO[40]	PULL_UP	LCD_D3	LCD_D3	1
EM_DAT4 / GPIO[41]	PULL_UP	LCD_D4	LCD_D4	1
EM_DAT5 / GPIO[42]	PULL_UP	LCD_D5	LCD_D5	1
EM_DAT6 / GPIO[43]	PULL_UP	LCD_D6	LCD_D6	1
EM_DAT7 / GPIO[44]	PULL_UP	LCD_D7	LCD_D7	1
EM_CMD / GPIO[45]	PULL_UP	LCD_D8	LCD_D8	1
EM_QS_N / GPIO[46]	PULL_UP	LCD_D9	LCD_D9	1
EM_QS_P / GPIO[47]	PULL_UP	LCD_D10	LCD_D10	1

POWER

Supply order	Supply	Default voltage	I _{max}	Default Enable	Usage
0	Buck1	1.15V	3000	On	VOC_MAIN, G2_VDD_1P0
1	LDO18	1.8V	200	On	VLDO_RF_1V8, VDDIC3_PMB12
2	Buck2	1.8V	1200	On	1.8V I/O, NAND LPDDR2(VDD1), LCD/TP I/O
3	Buck3	1.2V	1200	On	RF 1.2V, HSIC, LPDDR2(VDD2/VDDQ/VDDCA), VDD_CODEC
4	LDO1 LV	1.1V	200	On	G2_VDD_1P0 (Option reserved)
4	LDO3	2.8V	300	On	VLDO_RF_2V8
5	Buck4	1.8V	1200	On	VBUCK_RF_1V8
6	LDO7	2.8V	300	On	TBD
6	LDO5	3.1V	300	On	AVDD_USB
7	LDO14	2.8V	300	On	VOC_EMMC
0	Buck5	1.1V	1200	Off	RF APT
0	LDO6	2.8V	300	Off	WIB_3V3
0	LDO8	2.8V	300	Off	VOC_LCD_2V8, VDD_TP_2V8
0	LDO11	2.8V	300	Off	TBD
0	LDO9	1.8V	300	Off	WIB_1V8
0	LDO2 (I _{max} 10 mA)	2.0V	10	Off	MCBIAS_EXT
0	LDO 4	2.8V	300	Off	USIM1
0	LDO10	2.8V	300	Off	USIM2
0	LDO12	2.8V	300	Off	VOC_IO_MMC1
0	LDO13	2.8V	300	Off	VOC_SD CARD
0	LDO15	2.8V	300	Off	TBD
0	LDO16	2.8V	300	Off	TBD
0	LDO17	2.8V	300	Off	TBD
0	LDO19	2.8V	200	Off	V_GPS_1V8

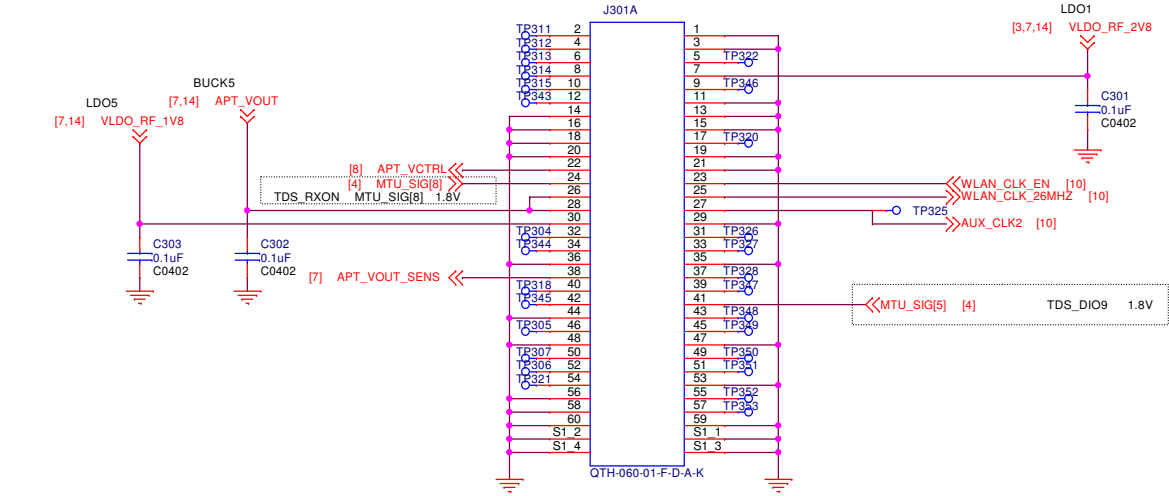
CLOCK



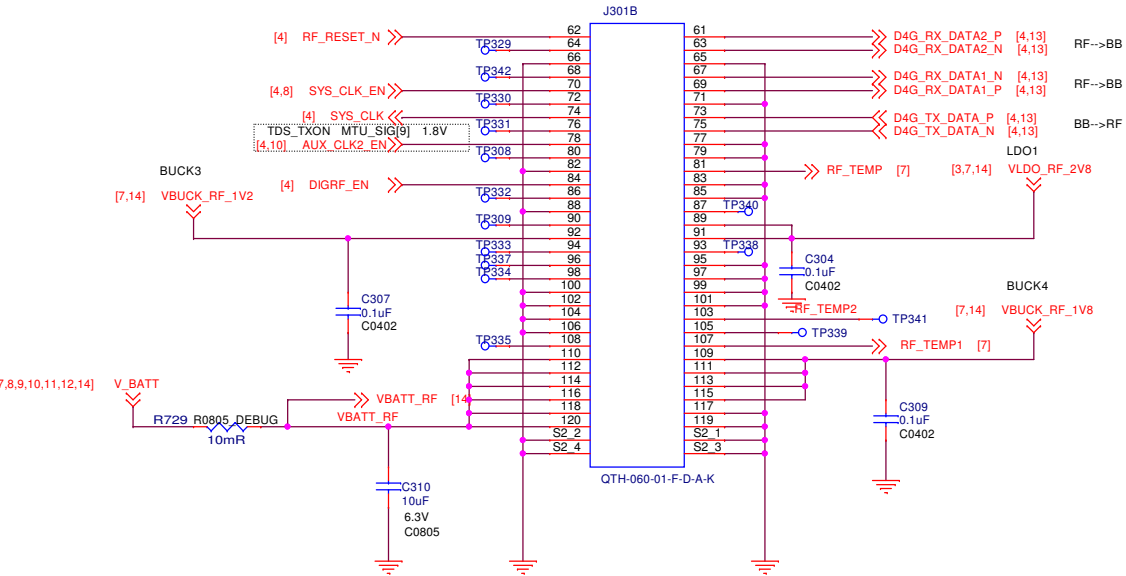
I2C

Device	PI2C (W/R)		CI2C (W/R)
PMB12	0x60/0x61, 0x62/0x63, 0x64/0x65, 0x66/0x67, 0x68/0x69, 0x6A/0x6B, 0x6C/0x6D, 0x6E/0x6F	CTP	0XB8/0XB9
BQ24193/BQ24192	0XD6/0XD7	OLED DISPLAY	0x7A/0x7B
PMB30	0XD1/0XD2		

RF CONNECTOR

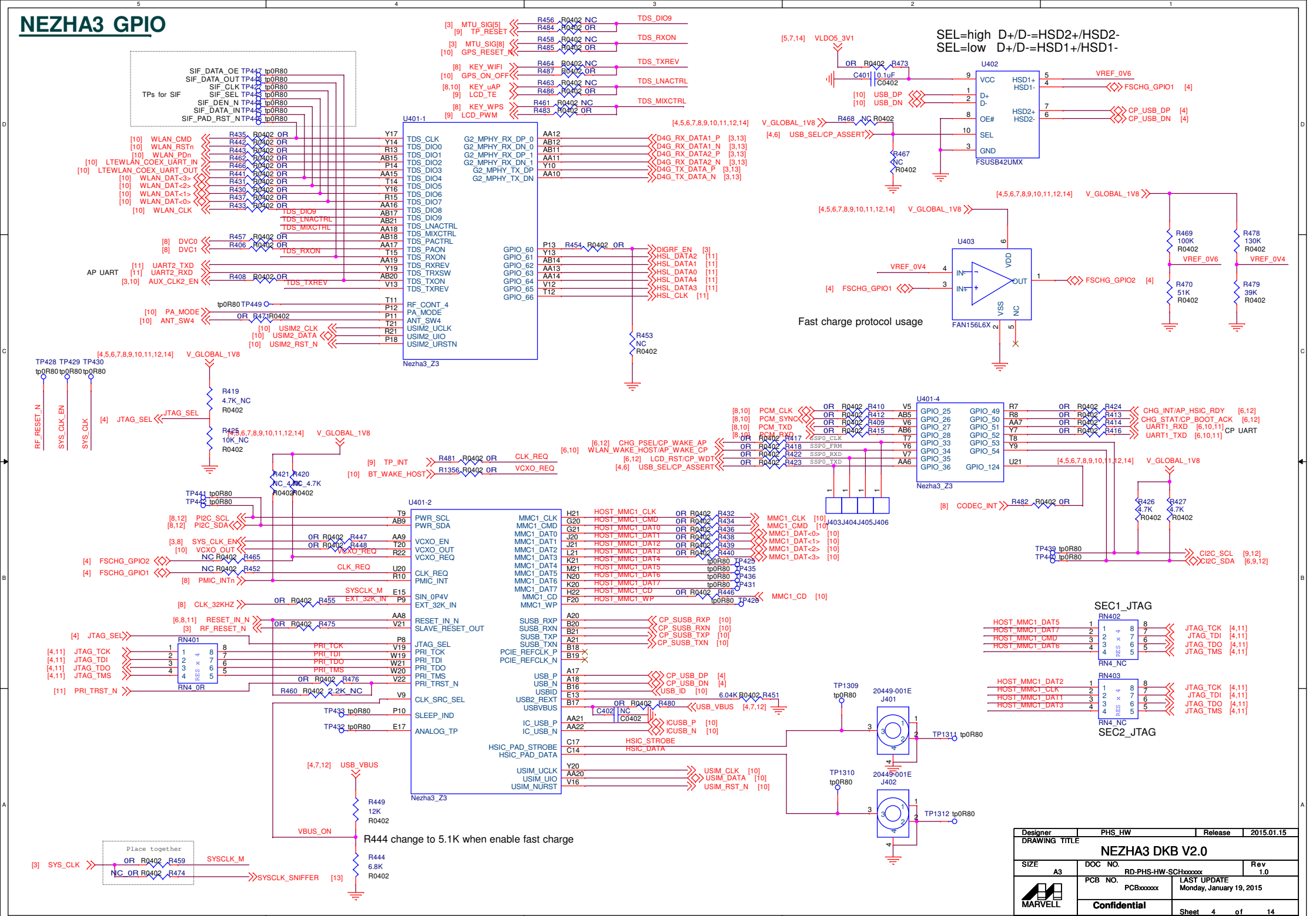


Dot box note:
MTU GPIOs reserved for CANARY RF CARD

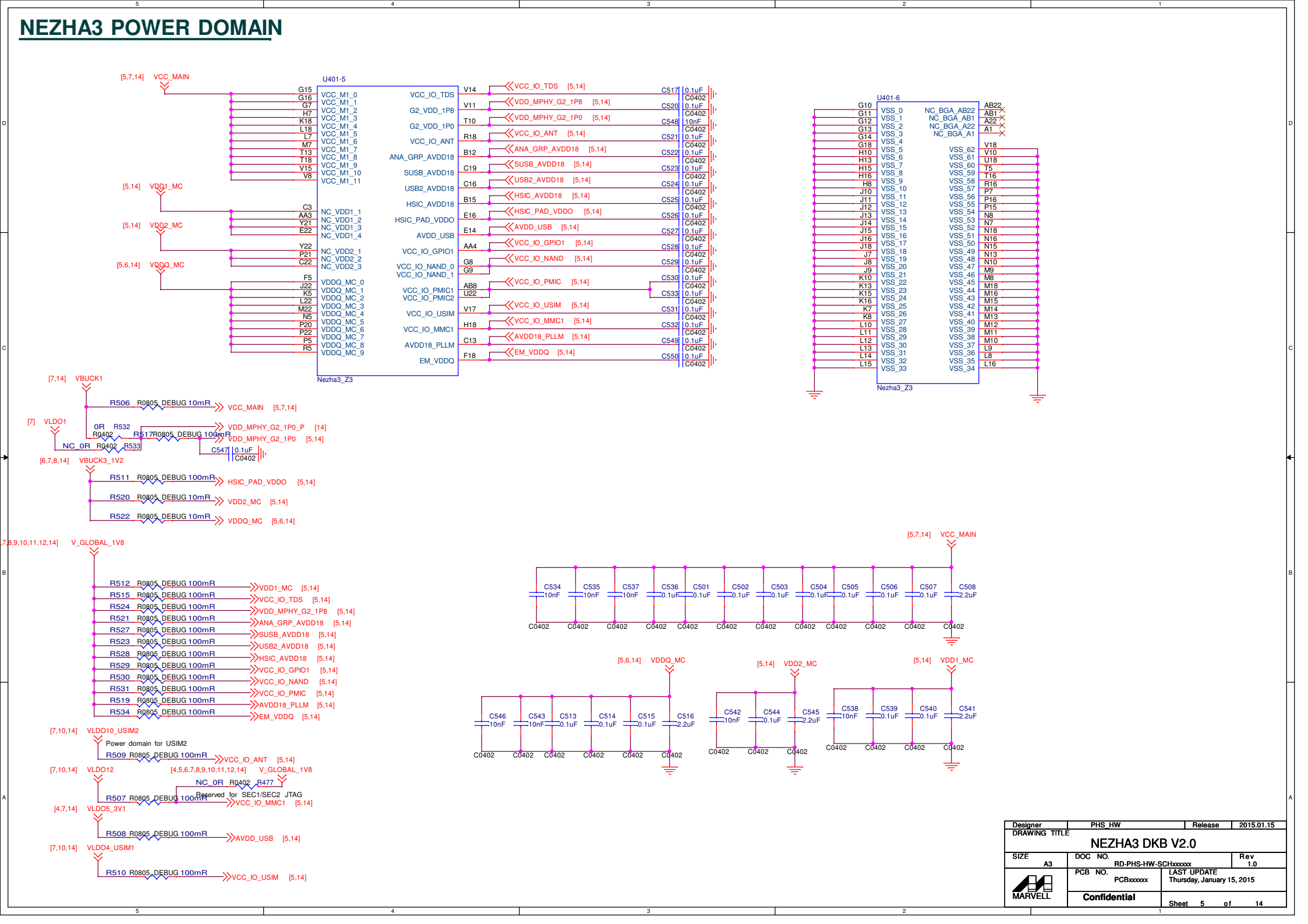


Designer	PHS_HW	Release	2015.01.15
DRAWING TITLE			
NEZHA3 DKB V2.0			
SIZE	DOC. NO.	Rev	
A3	RD-PHS-HW-SCHxxxxx	1.0	
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NEZHA3 GPIO

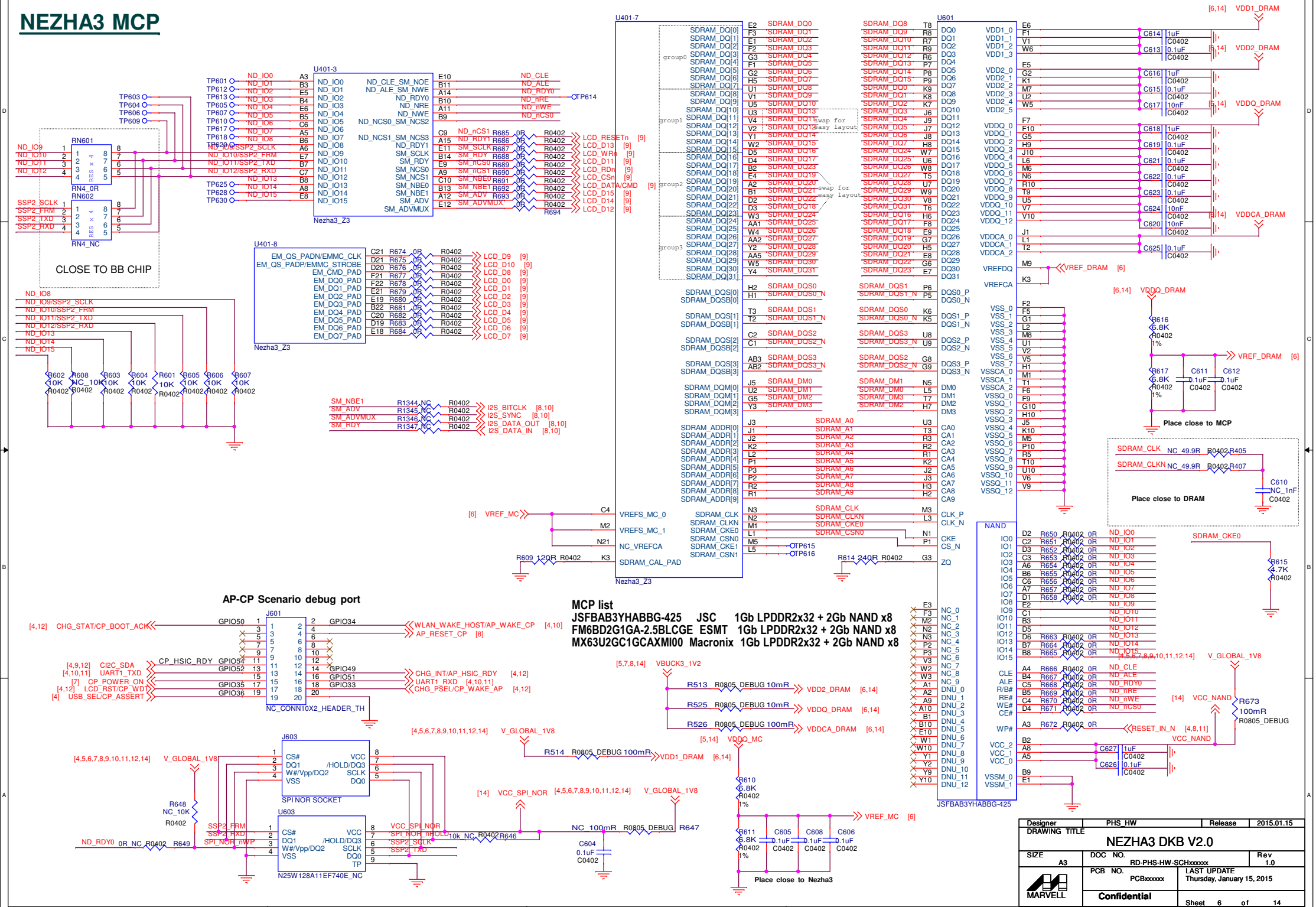


NEZHA3 POWER DOMAIN

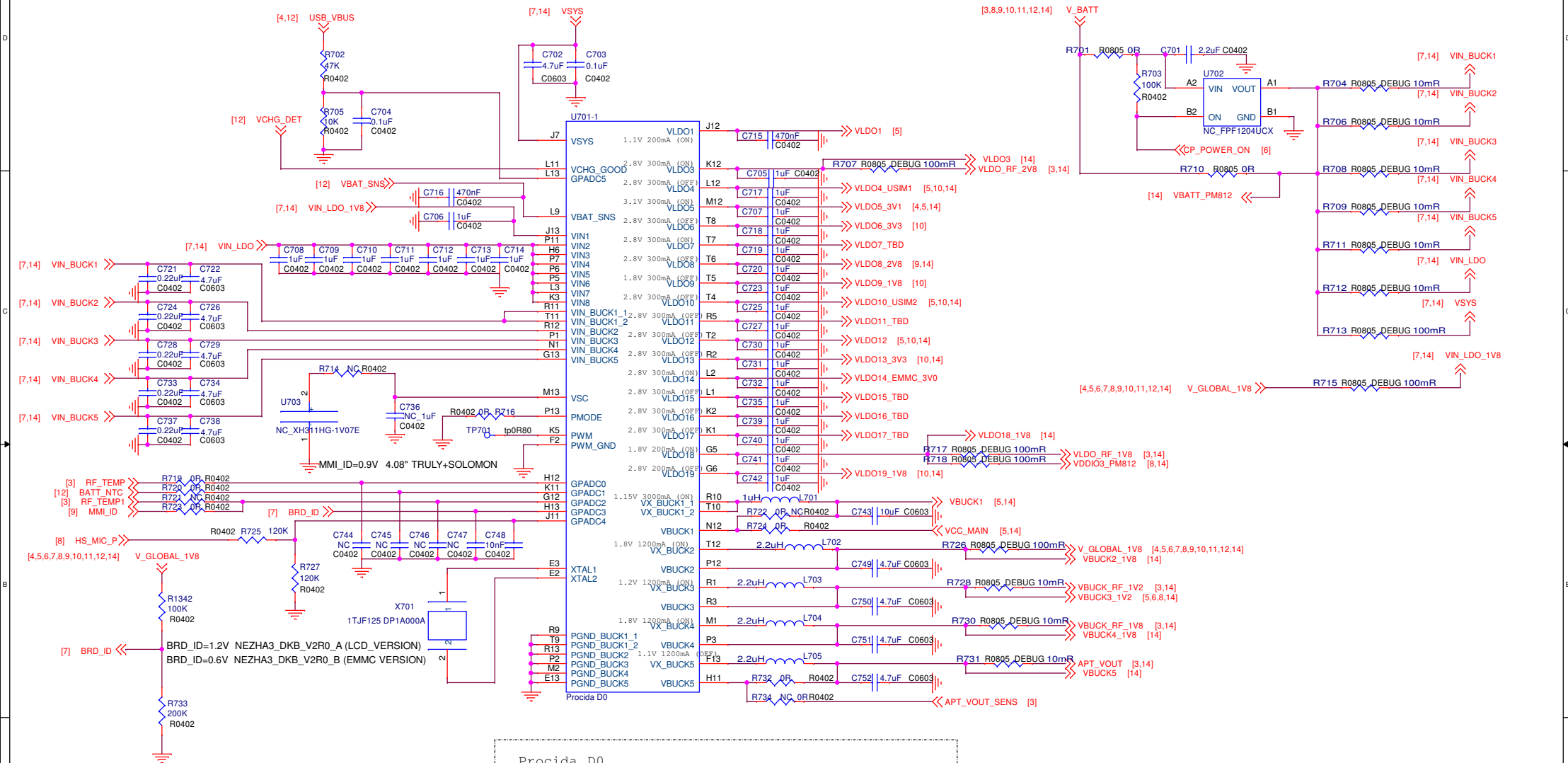


Designer	PHS_HW	Release	2015.01.15
DRAWING TITLE			
NEZHA3 DKB V2.0			
SIZE	A3	DOC NO.	RD-PHS-HW-SCHxxxxx
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NEZHA3 MCP




PM812 POWER SUPPLY



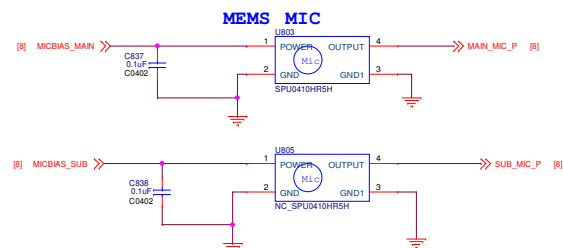
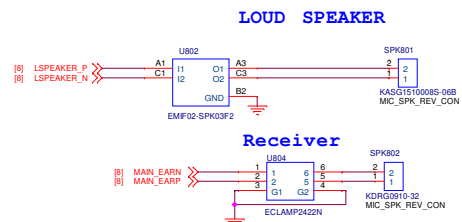
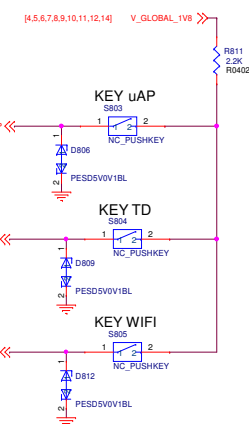
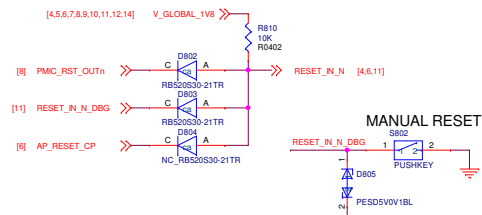
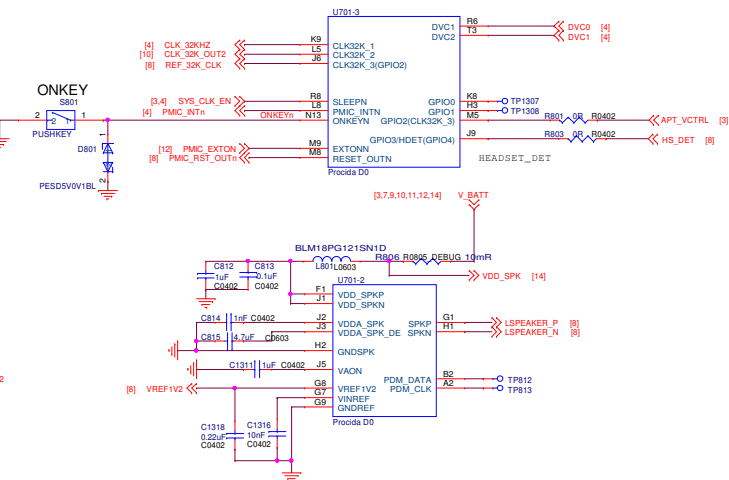
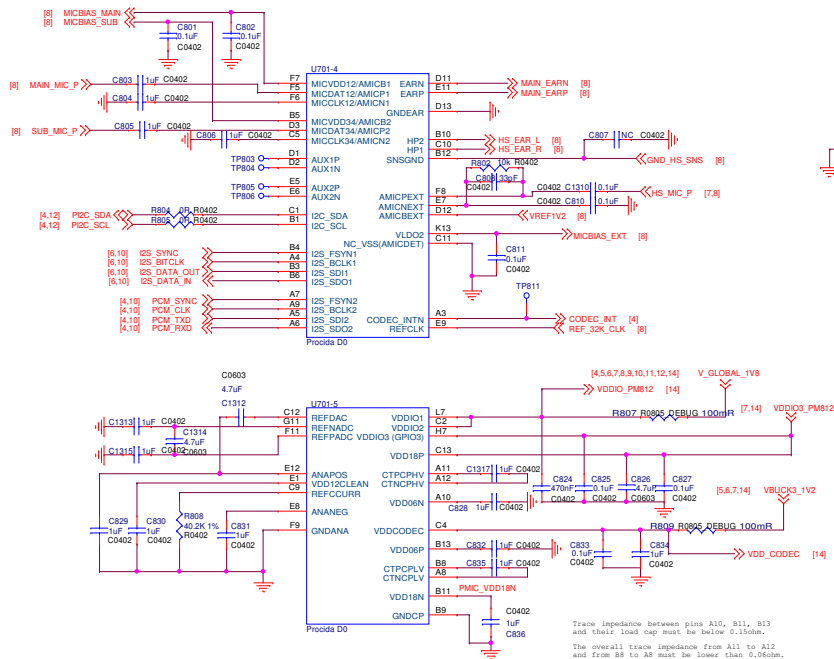
Procida D0

```
I2C   address:0x60/0x61,0x62/0x63,0x64/0x65,0x66/0x67,
0x68/0x69,0x6A/0x6B,0x6C/0x6D,0x6E/0x6F,0x70/0x71
```

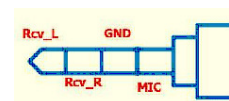
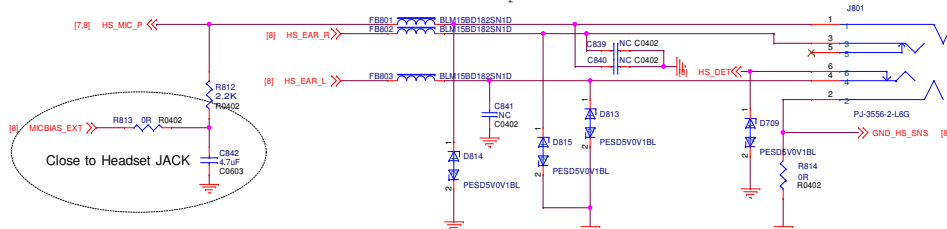
PLATFORM MODE: 0x0


Designer	PHS_HW	Release	2015.01.15
DRAWING TITLE			
NEZHA3 DKB V2.0			
SIZE	DOC NO.	Rev	
A3	RD-PHS-HW-SCHxxxxxx	1.0	
	PCB NO.	LAST UPDATE	
	PCBxxxxxx	Tuesday, January 20, 2015	
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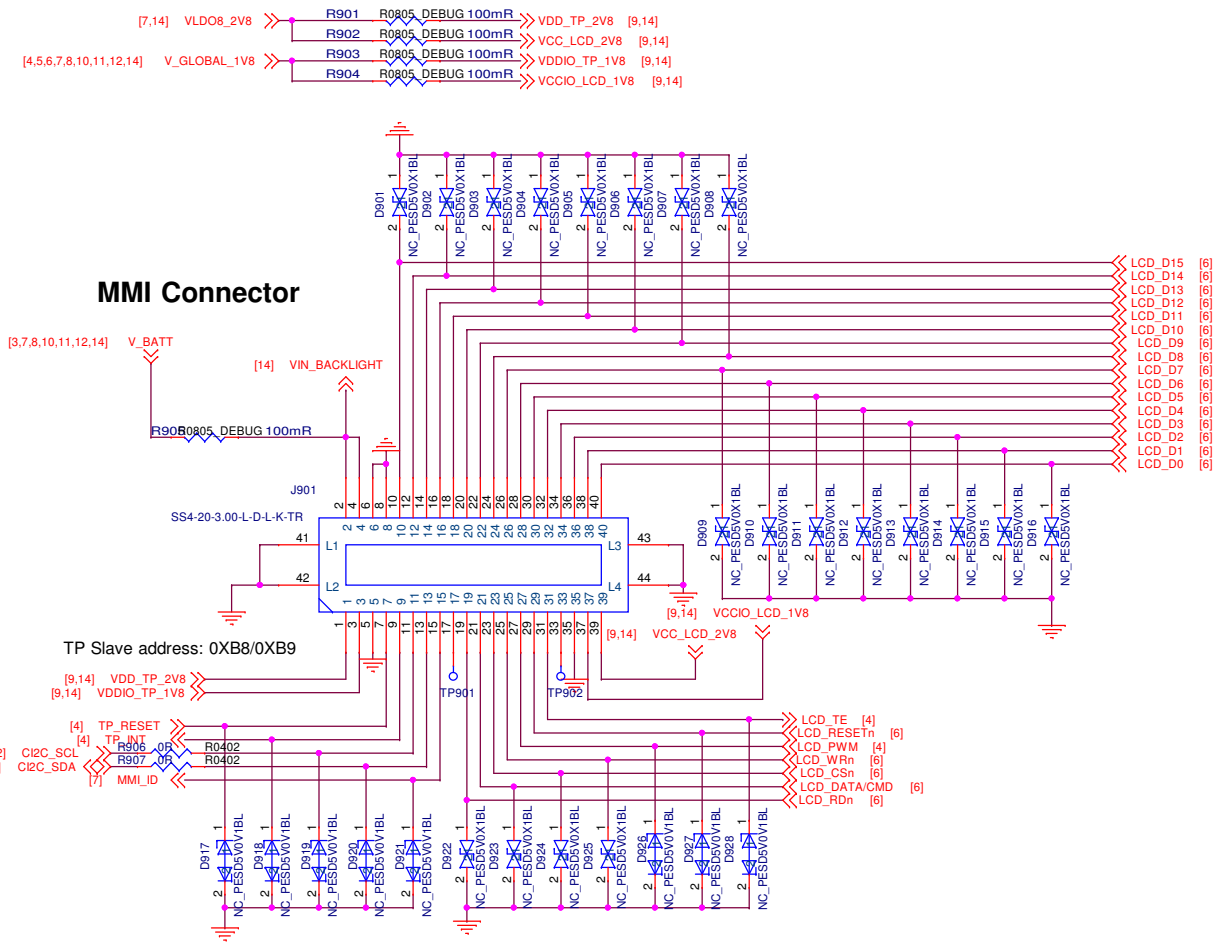
PM812 MSIC/AUDIO CODEC




3.5" Earphone Connector
compatible with MOTO and APPLE

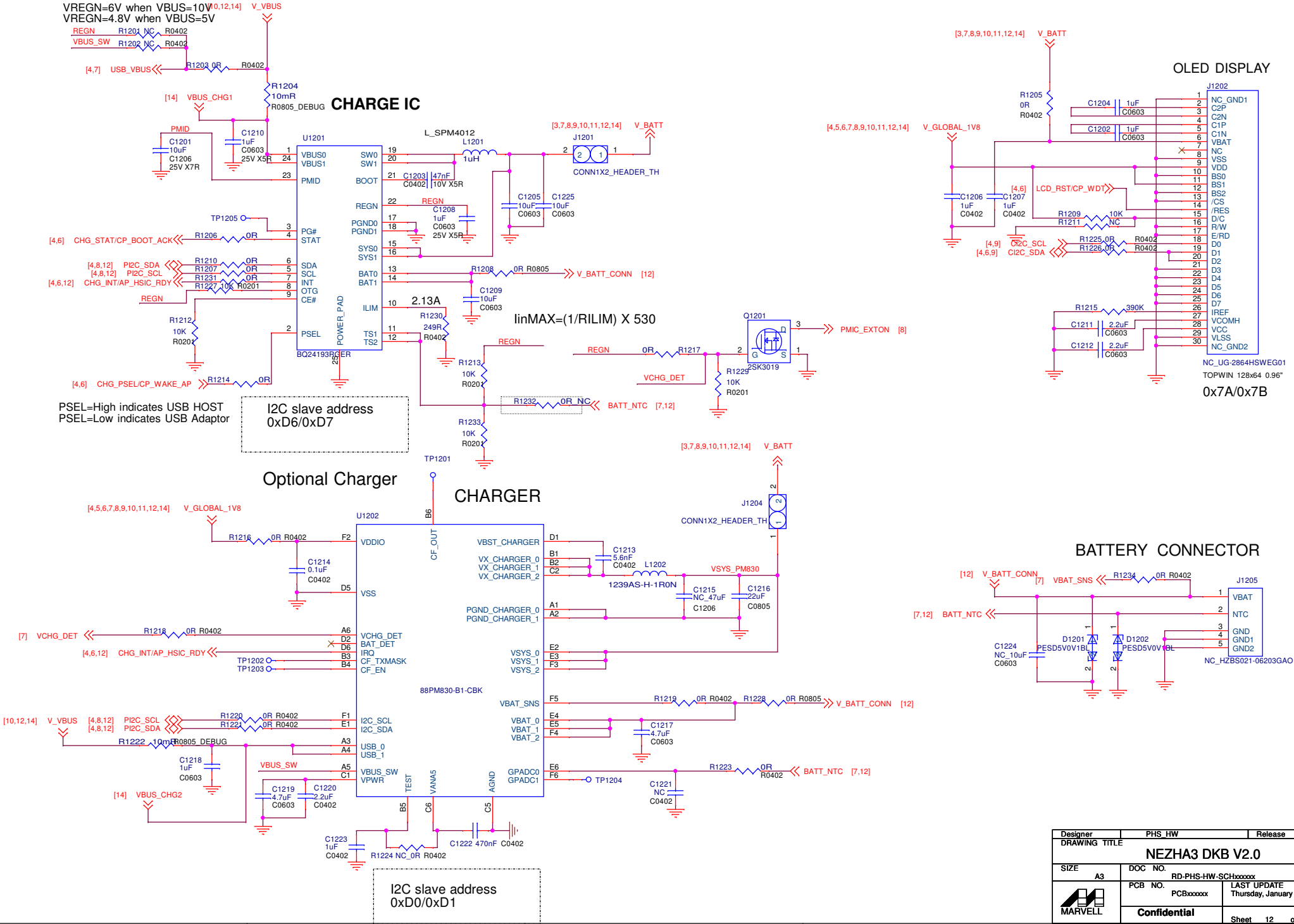


Designer	PHS HW	Release	2015.01.15
DRAWING TITLE			
NEZHA3 DKB V2.0			
SIZE	DOC NO.	Rev	
A2	RD-PHS-HW-SCH000000	1.0	
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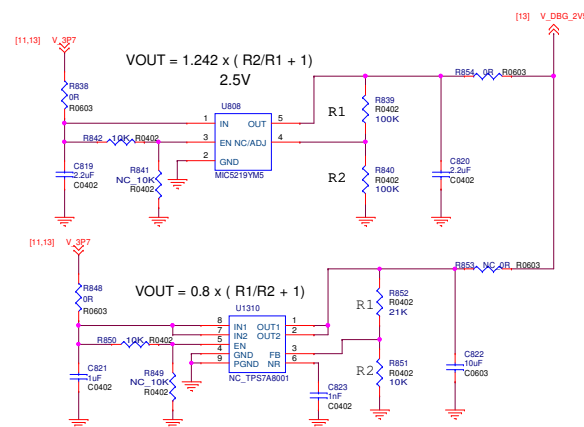
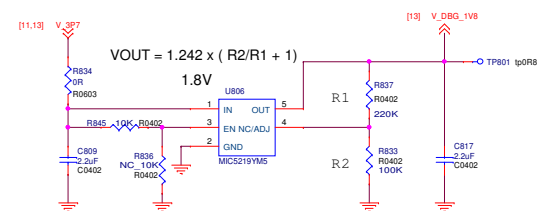
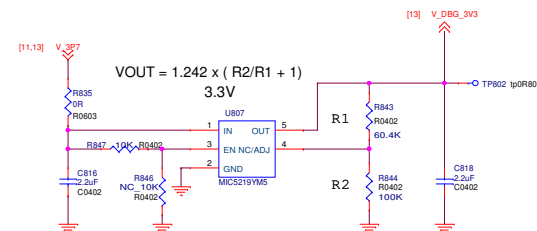
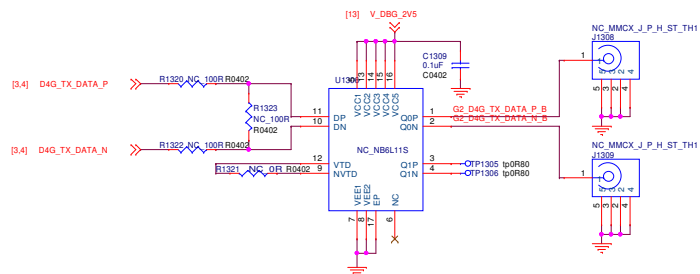
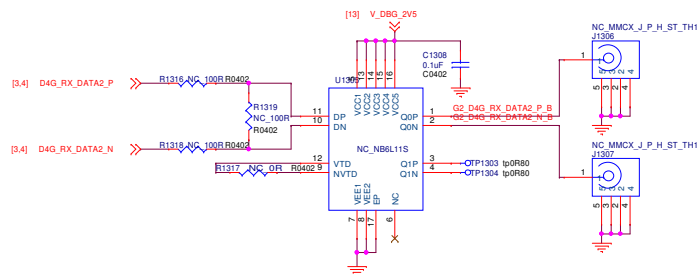
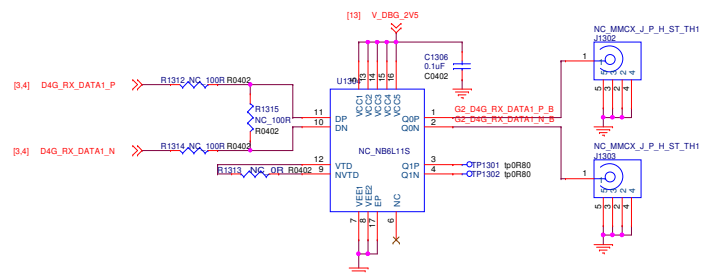
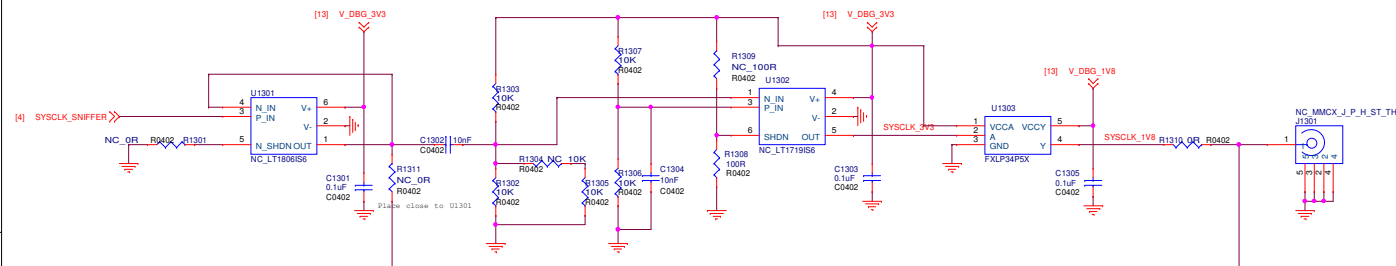
Designer	PHS_HW	Release	2015.01.15
DRAWING TITLE			
NEZHA3 DKB V2.0			
SIZE	DOC NO.	Rev	
A3	RD-PHS-HW-SCHxxxxx	1.0	
	PCB NO.	LAST UPDATE	
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CHARGER/OLED DISPLAY

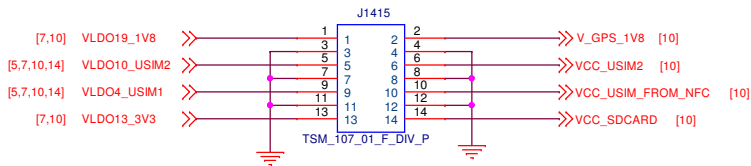
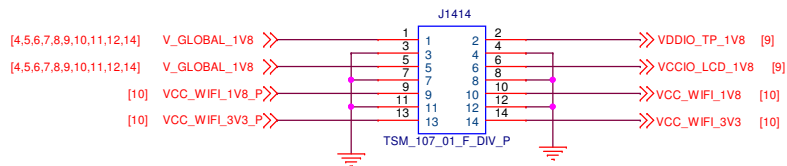
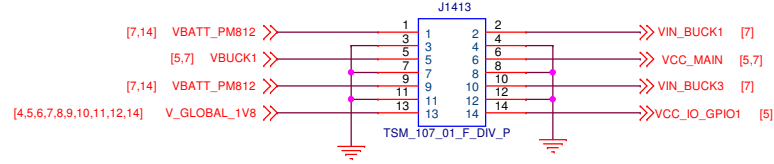
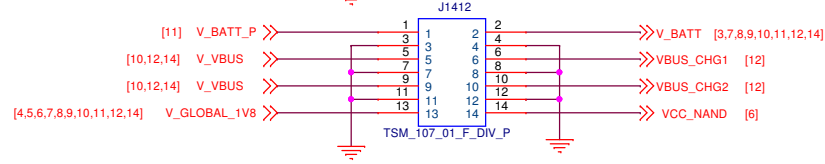
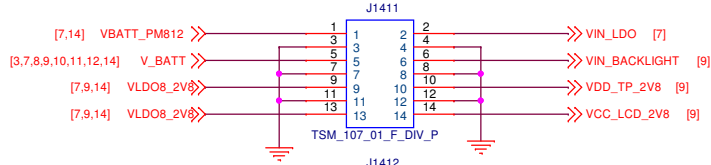
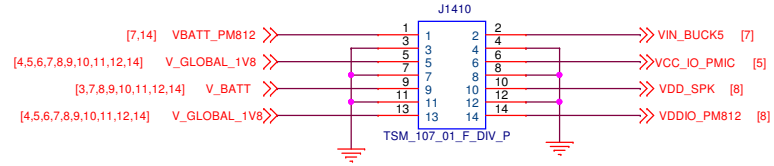
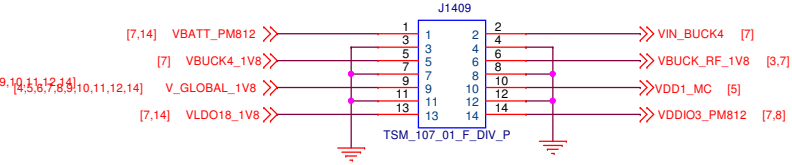
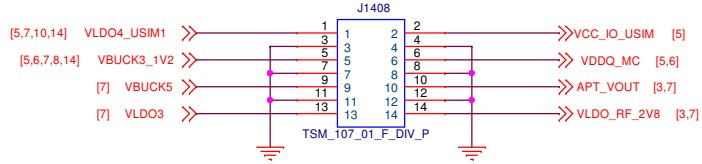
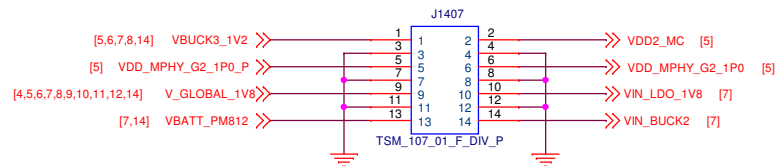
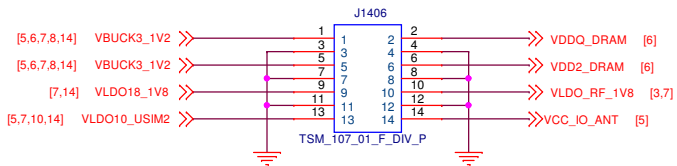
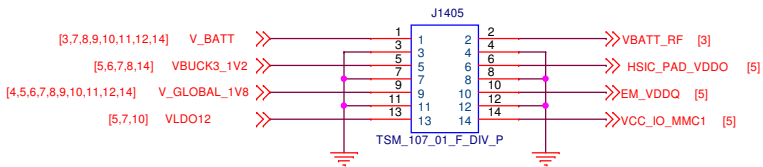
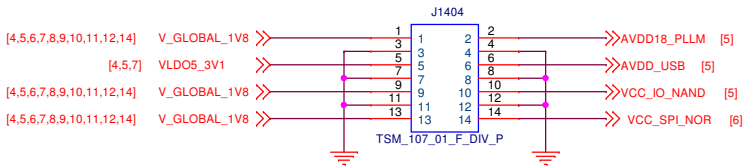
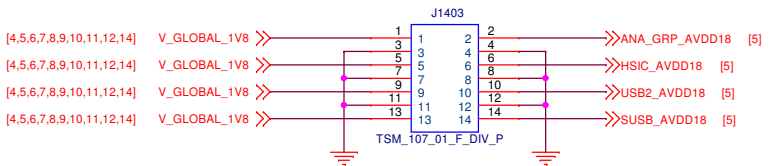
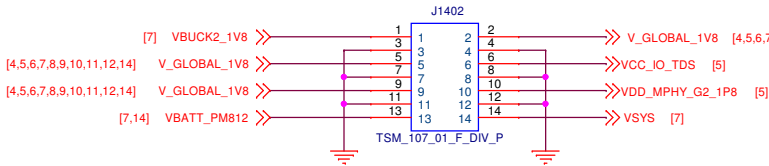
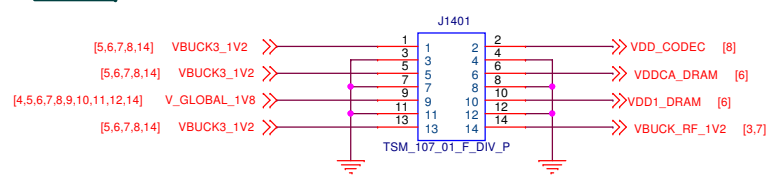


Designer	PHS_HW	Release	2015.01.15
DRAWING TITLE	NEZHA3 DKB V2.0		
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DRAWING TITLE				
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A2	RD-PHS-HW-SCH000000		1.0	
	PCB NO.		LAST UPDATE	
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DRAWING TITLE			
NEZHA3 DKB V2.0			
SIZE	A3	DOC. NO.	RD-PHS-HW-SCHxxxxx
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